ABSTRACT OF THE DISCLOSURE

An I/O interface circuit immediately close to a bank having a plurality of memory cells and an I/O circuit is directly connected to data line pairs via a switching circuit. Another I/O interface circuit is connected to other data line pairs via switching circuits and data bus pairs. Consequently the number of lines of the data bus pairs provided within the chip of the semiconductor integrated circuit is half of the number in the prior art, and the chip area can be reduced.